

ABSTRACT OF THE DISCLOSURE

One embodiment of a system for disabling a computer bus upon detection of a power fault includes a bus bridge device coupled to a bus and a power regulator that delivers power to the bus. If the power regulator detects a power fault, then the power
5 regulator asserts a fault signal to the bus bridge device. The power regulator also removes power from the bus. The bus bridge device disconnects an internal logic unit from the bus in response to the assertion of the fault signal. The bus bridge device, in further response to the assertion of the fault signal, alerts the system of the power fault by asserting an interrupt signal.

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